WHAT IS CLAIMED IS:

1. A method of reducing impedance variations in an electrical circuit configured for placement on an integrated circuit (IC) substrate, the electrical circuit including an electrical component having (i) input and output ports and (ii) a plurality of cascaded impedance devices configured for connection along a feedback path formed between the input and output ports, each impedance device having a predetermined impedance value, the method comprising:

forming sets of parallel connected resistors, each set (i) corresponding to one of the impedance devices, (ii) including two or more parallel resistor paths, and (iii) having a total impedance value substantially equal to the predetermined impedance value of its corresponding impedance device; and

configuring the sets of parallel resistor paths to form an interdigital structure across the substrate when the electrical circuit is placed thereon, the interdigital structure being formed when the parallel resistor paths split at one point on the substrate and recombine at another point.

2. An apparatus for reducing impedance variations in an electrical circuit structured and arranged for placement on an integrated circuit (IC) substrate, the electrical circuit including an electrical component having (i) input and output ports and (ii) a plurality of cascaded impedance devices configured for connection along a feedback path formed between the input and

output ports, each impedance device having a predetermined impedance value, the apparatus comprising:

means for forming sets of parallel connected resistors, each set (i) corresponding to one of the impedance devices, (ii) including two or more parallel resistor paths, and (iii) having a total impedance value substantially equal to the predetermined impedance value of its corresponding impedance device; and

means for configuring the sets of parallel resistor paths to form an interdigital structure across the substrate when the electrical circuit is placed thereon, the interdigital structure being formed when the parallel resistor paths split at one point on the substrate and recombine at another point.

3. The apparatus of claim 2, wherein the electrical component is a programmable gain amplifier (PGA).

4. The apparatus of claim 3, wherein the PGA is a differential amplifier.

5. The apparatus of claim 4, wherein the predetermined impedance values of all of the impedance devices are substantially equal.

6. The apparatus of claim 5, wherein the IC is formed in CMOS.